REMARKS

Claims 1-14, 16-22, 24-30 and 32-34 are pending. Claims 1, 2, 7, 12, 16, 20, 21, 22, and 32 are amended, claims 15, 23, and 31 are canceled, and claims 33 and 34 added with this response. Reconsideration of the application in light of the above amendment and the following remarks is respectfully requested.

I. CLAIM OBJECTIONS

Claims 2, 7, 12, 16, 21, and 22 were objected to for informalities leading to lack of antecedent basis. Claims 2, 7, 12, 16, 21, and 22 are amended herein to address the highlighted informalities.

Accordingly, withdrawal of the objections is respectfully requested.

II. EXPLANATION OF THE AMENDED CLAIM LANGUAGE

It is to be appreciated that while reference may be made back to certain parts of the application in this Reply (*e.g.,* page numbers, line numbers, figures, etc.), that such referencing is not to be interpreted in a limiting manner (*e.g.,* to limit the scope of the claims and/or features therein to the particular portion(s) referenced), but is instead merely done for purposes of explanation, illustration and/or ease of understanding.

Independent claim 1 provides a method of transferring data entries from a peripheral to a data queue in a host memory, the method comprising, determining a lower limit on a number of available data entry positions in the data queue and selectively transferring a current data entry to the data queue if the lower limit is greater than or equal to a first value. The lower limit in this regard may be related to a number of available data entry positions in the data queue or possibly the number of unused incoming data status entry positions. (*See, e.g,* applicant's specification, page 5, lines 22-25). A first value is a number related to the current cache line size. Figure 6 illustrates cache 115 where the cache line length is equal to 64 bytes. Status entries 199 located in host system memory 128, illustrate that the status entries are 8 bytes long, as one example. Accordingly, a single cache line can accommodate up to 8 status

entries. Therefore claim 1 provides, if the unused incoming data status entry positions (the lower limit) is greater than some predetermined value (i.e., the first value that is associated with a full cache line size), for example, then the current data entry is selectively transferred to the data queue.

Currently amended claim 16 provides for a further limitation of claim 2, wherein the remaining portion of the data queue after receipt of the current incoming data status entry and any previous incoming data status entries is padded so as to equal a length of a full cache line. Figure 7A-7D illustrates this limitation in further detail. Figure 7 A illustrates current cache line 132b, where no status entries 199 have been written, thus leaving 8 free unused status entry positions. (*See, e.g,* page 23, line 7-8). Figure 7B illustrates a status entry 199a has been written to the memory 128 and to the current cache line copy 132b, with 7 unused status entry positions that are padded to a full cache line size. (*See, e.g,* page 23, lines 12-14). Figures 7C-7D illustrates further addition of status entries to the current cache line copy.

New claims 33 and 34 and amended claim 31 provide similar limitations as discussed above with the addition of language that describes the selectively transferring of data in full cache line lengths. These amendments are supported further in the Detailed Description of the Invention.

III. REJECTION OF CLAIMS 1, 2, 16, 20-22, and 24-32 UNDER 35 U.S.C. § 112

Claims 1, 2, 16 and 20-22, and 24-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 20 and 22 are rejected for lack of antecedent basis. Claims 3-19 and 22-32 are rejected for incorporating the defects of the claims from which they depend. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 1, 2, 16, 20, 21, 22, and 31 have been amended with the removal of the indefinite terms “full cache line write” and “partial cache line write”.

Additionally, claim 20 has been amended to replace "the data queue" with "the host memory" and claim 22 has been amended to provide sufficient antecedent basis. Claims 3-14, 16-19, 22, and 24-32 depend upon claims 1, 2, 20, and 21 which are now believed to be in compliance with 35 U.S.C. § 112, thus bringing the dependant claims into compliance as well.

Accordingly, withdrawal of this rejection is respectfully requested.

IV. REJECTION OF CLAIMS 1-32 UNDER 35 U.S.C. § 103(a)

Claims 1, 20 and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,212,593 B1 (Pham), in view of U.S. Patent No. 5,491,811 (Arimilli) and U.S. Patent No. 5,586,297 (Bryg). Claims 2-19 and 22-32 are rejected under 35 U.S.C § 103(a) as being unpatentable over Pham, Arimilli, and Bryg as applied to claims 1, 20, and 21 above, and further in view of U.S. Patent No. 6,212,593 B1 (Garrett). Withdrawal of these rejections is respectfully requested for at least the following reasons.

i. Pham does not teach selectively transferring a current data entry to the data queue.

Claims 1, 20, and 21 provide a system and method of transferring data entries from a peripheral to a data queue in a host memory by selectively transferring a current data entry to the data queue. Consequently, the transfer of the current data entry to the data queue only occurs if a condition is met. As will be further appreciated from the following discussion, Pham does not teach selectively transferring a current data entry to the data queue.

The Office Action dated December 12, 2008 (FOA) asserts Pham teaches selectively transferring a current data entry to the data queue, with reference to setting a start of packet value (STP, 258) and an end of packet value (ENP, 260). (*See, e.g.,* FOA, page 8, sec. c). As taught by Pham, the setting of the STP (258) indicates that

the corresponding buffer is the first buffer to be used for a corresponding packet. (*See, e.g.,* Column 7, lines 53-67). The implementation of the STP (258) ***allows for chaining together of multiple buffers*** to transmit a single packet. Correspondingly, ***the ENP (260) indicates the last buffer used in the chain for the packet***. If for instance both values are set to true, then it can be reasoned that the packet fits into a single buffer, this however does not mean Pham teaches that the packet was transferred **selectively** to the buffer, as claimed. ***What Pham does teach is that a packet of varying size can be stored in a plurality of buffers and transferred accordingly, without regard to selectively transferring a current data entry to the data queue.***

Therefore independent claim 1, 20, and 21 along with respective depending claims 2-14, 16-19, 21, 22, and 24-32 are believed non-obvious over Pham and thus allowable. Accordingly withdrawal of the rejection is respectfully requested.

ii. Pham does not teach selectively transferring a current data entry to the data queue if the lower limit is greater than or equal to a first value.

Similar to the discussion above, claim 1, 20, and 21 provides for transferring data entries from a peripheral to a data queue in a host memory, the system and method comprising selectively transferring a current data entry to the data queue if a lower limit is greater than or equal to a first value. It is respectfully submitted, Pham does not teach selectively transferring a current data entry to the data queue if the lower limit is greater than or equal to a first value.

Pham teaches the packet (current data entry) can span a number of data buffers (data queues) and is processed according to the STP bit (256) and the ENP bit (260). (*See, e.g.,* FOA, page 9, sec. c). ***The establishment of the STP bit (258) and ENP bit (260), as taught by Pham, allows for spanning a packet larger than a single buffer, thus precluding the need to fit a packet into an appropriately sized buffer.*** The transmit terminal count interrupt enable bit value (TTCE), as taught by Pham, provides

for buffer-by-buffer interrupt control according to the invention. (*See, e.g.,* col. 7, line 66-col. 8,line 11). According to the cited reference, Pham teaches when TTCE value 262 is 0, it disables interrupts on completion of the buffer and when set to 1 an interrupt is issued on the completion of the transmission of the corresponding buffer. The description of the TTCE value 262 is further illustrated in Fig. 7 and box 506, as suggested by the FOA. Fig. 7 and box 506 illustrates a middle buffer state where both the STP bit 258 and the ENP bit 260 are both false, and after the 20 bytes of the corresponding buffer 206 are transmitted, no transmit on terminal count interrupt is generated because the TTCE bit 262 is false. (*See, e.g.,* column 12, lines 61-66).

As detailed by the preceding discussion and the reference prescribed by the FOA, Pham does not teach selectively transferring a current data entry to the data queue if the lower limit is greater or equal to a first value. ***According to Pham, the data entry is transferred to the data queue unconditionally. The only conditions taught, by this reference to Pham, are placed on interrupts being placed indicative of the full reception of the packet, as indicated by STP 258, the ENP bit 260, and the subsequent setting of the TTCE bit 262.*** All which provide no indication or condition on a lower limit as compared to a first value.

Therefore independent claims 1, 20, and 21 along with respective depending claims are believed non-obvious over Pham and thus allowable. Accordingly withdrawal of the rejection is respectfully requested.

V. NEW CLAIMS 33-34

Claims 33-34 have been added herein and are believed to be allowable over the cited art.

VI. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP769US.

Respectfully submitted,
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